Two different approaches of power-integrity analysis and correlation with on-chip measurement

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1. Introduction

Supply voltage noise had become a major problem for high performance/efficiency processor design, it was generated by various sources. The noise caused by interaction between on-die current draw and chip/package/board RLC resonance usually dominate in advance high performance processor.

Traditionally, chip and system (package and board level) designer were worked in two different camps, each has clear voltage noise budget requirement given to them, the full system power requirement would be met when two camp of designers both meet the given budget. As chip technology moved to advance technology node, high current density on chip side and smaller overall package dimension result in greater RLC noise that stretch this concept of divide and conquer to a point that the traditional methodology was no longer practical. During chip development, chip designers need robust flow that consider package and board effect, in the meantime while concurrently develop with chip, package and board designers also need a flow to consider chip behavior.

In this presentation, we proposed two different supply noise simulation flow, one from chip designer's point of view and the other from package/board designer's point of view. These two simulation flow were tuned to reduce miss-correlation between each other.

To make sure there's no significant modeling error, on-die high bandwidth voltage sensors were used for final silicon correlation.

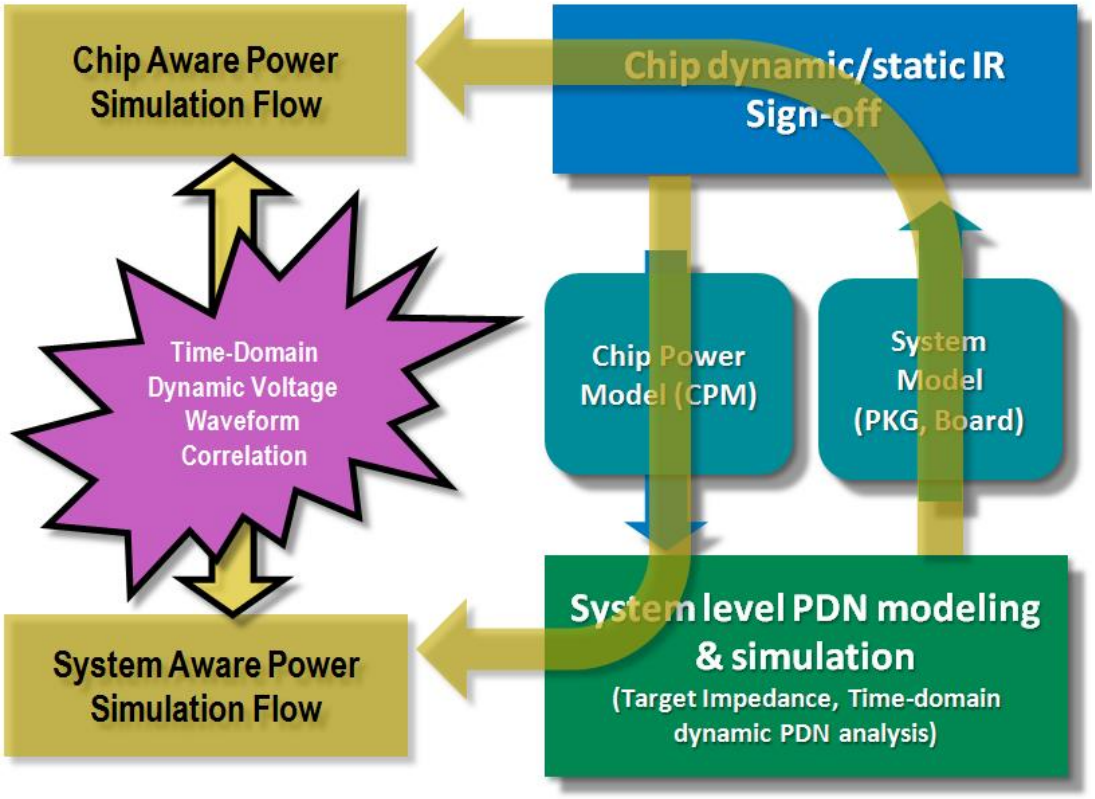


Figure 1. The curved arrow shows 2 types of power simulation flow, the analysis view from system level and the analysis view from chip level.

2. Modeling and Simulation

Chip level modeling

1. Use gate-level, true-time FSDB pattern.
2. CPM models were used to model chip in system level power integrity analysis, CPMs were composed of:
   - Header: chip package protocol (CPP) include pad location information for the connection between chip and Package.
   - Parasitic: spice compatible lump RLGC model with total >100 nodes that includes on-chip un-gated and gated power network.
   - Current model: Per-bumps current waveform with global ground node based on cell level timing and dynamic current consumption.

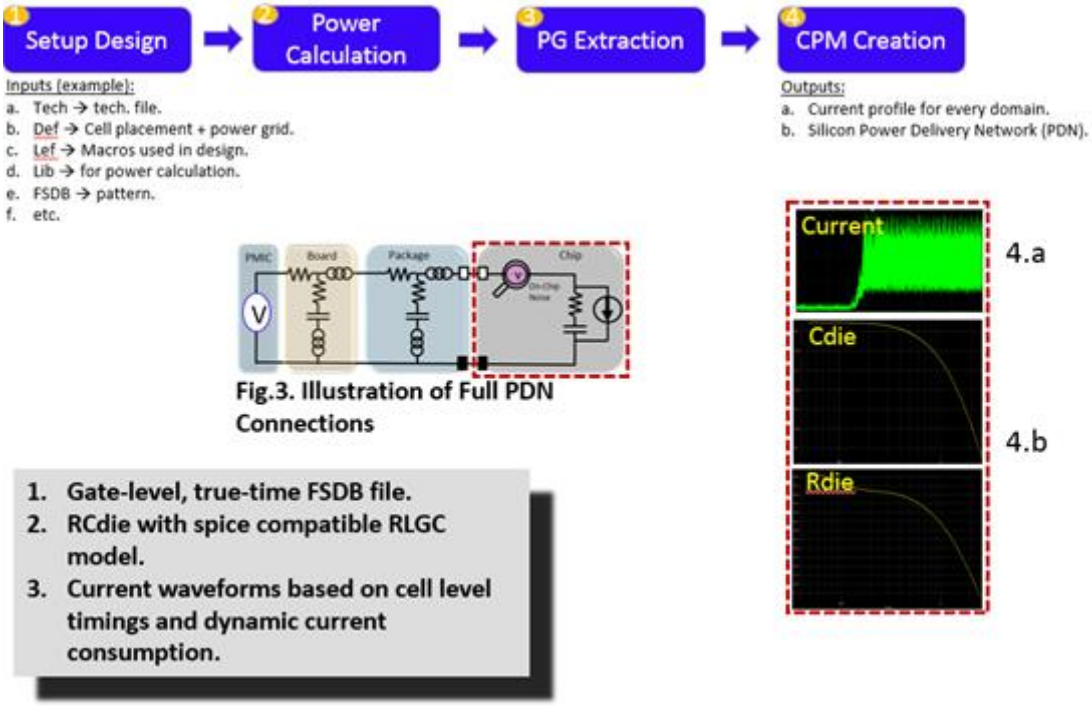


Fig.3. Illustration of Full PDN Connections

Fig2. CPM Generation Flow

Package / Board Modeling

- **Package modeling:**
  - Per-bump resolution SPICE model includes nodes of decoupling capacitors. Parasitic are associated with every bump.
  - CPM contains the IC die power model and pin location (ploc). PLOC information enables PKG extraction tool to automatically align and connect the IC die pins and the package pins.
  - PKG model was extracted by ANSYS SIwave-CPA Q3D solver. It also supports 3D FEM-based solver extraction of power nets on package. (The theory of operation of different solver will be presented on next page)
- **PCB modeling:**
  - Using hybrid solver to extract board level power delivery network and export S-parameter which includes DC information and on-board de-coupling capacitors.

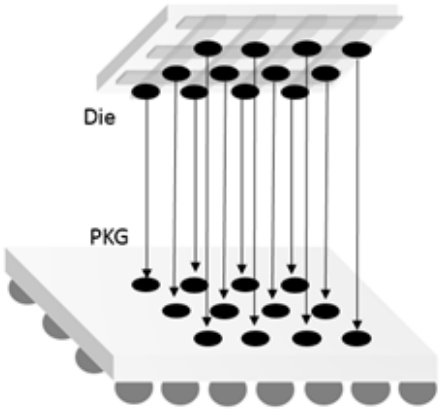
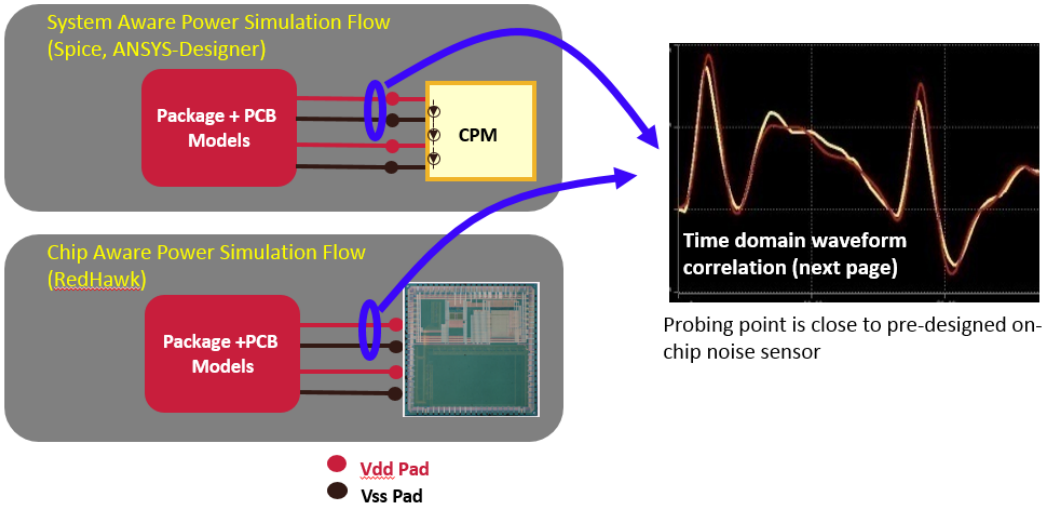


Fig 3. System (Package/Board) level modeling.

Voltage waveform comparison between system and chip aware power simulation flows



Probing point is close to pre-designed on-chip noise sensor

Fig 4. Correlation between chip and system aware power simulation.

3. Silicon measurement

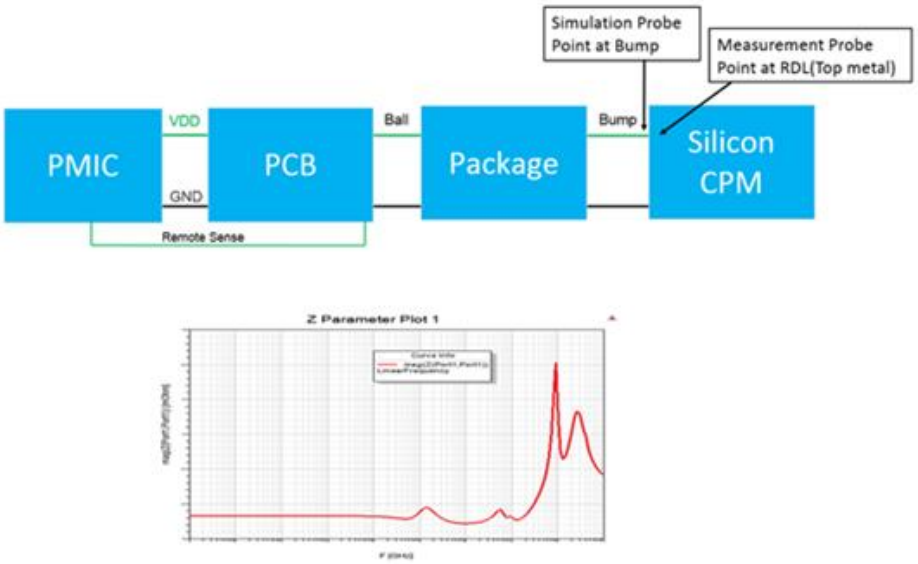


Fig 5. Silicon probe point and PDN Z Parameter Plot.

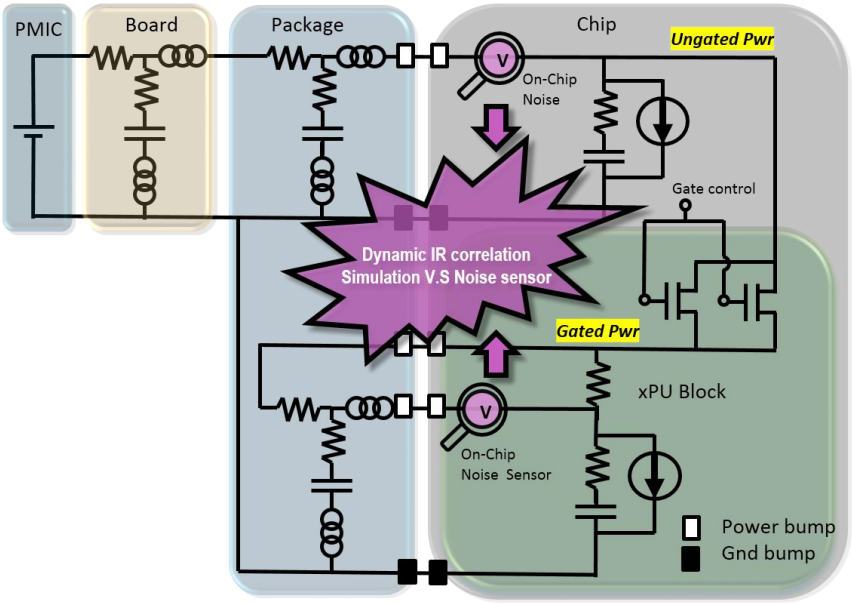
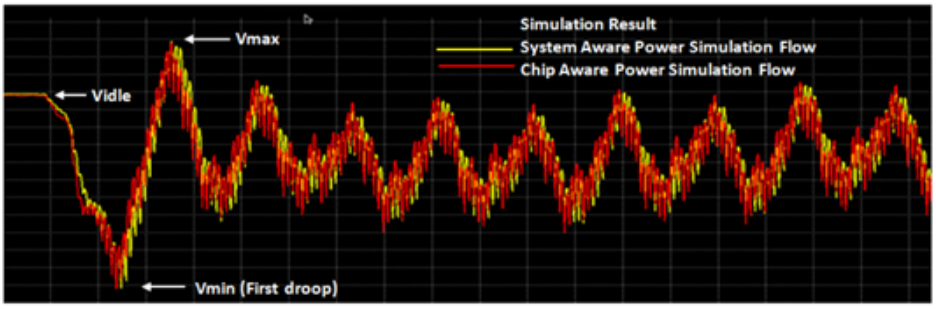


Fig 6. Complete system PDN model and on-die noise sensing points.

4. Conclusion and Future works

- The simulation result between two power simulation flows correlated well.



- The correlation between simulation and on-die noise sensor measurement.
  - On-die noise sensor used comparator circuitry to detect voltage droop by comparing programmable Vref and VDD.

Main Idea	Normalized Delta to Msmt
1	0.95%
2	1.05%

Fig 7. Correlation between chip aware, system aware simulation and on-die measurements.

- **In this study we demonstrates two different simulation approaches for power integrity analysis from chip and system design perspective. The result shows that with correctly tuned flow, approaches from chip and system side can correlate well.**
- **This study also shows voltage correlation between simulation and on-die sensor measurement to within 1.05% normalized difference.**
- **Future works: simulation time and accuracy improvements.**
  - **Higher pattern coverage slowed down CPM and on-chip IR simulation time.**
  - **Higher number of CPM ports slowed down transient simulation time drastically.**
  - **Measurement with transient waveform at bump instead of measurement with discrete value (Vmin) through Comparator to improve accuracy.**